FPGA-BASED COMPENSATOR OF HYSTERETIC ACTUATOR NONLINEARITIES FOR HIGHLY DYNAMIC APPLICATIONS

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Abstract:
A method developed at the Laboratory of Process Automation (LPA), Saarland University, for compensating complex hysteretic actuator and sensor characteristics in open loop control is based on the so-called modified Prandtl-Ishlinskii method. Within the scope of the EU-funded project MESEMA (contract AST3-CT-2003-502915) the algorithm for the inverse filter was implemented in a FPGA and a digital circuit was developed, which can compensate two hysteretic actuator characteristics independently and simultaneously in open loop control, or one inverse filter can be integrated in a closed control loop, i.e. the second channel can be used for the feedback implementation. This board is easily extendable to several channels, since the FPGA works below its full capacity and other control algorithms could be implemented. The signal digitising occurs with 14 bit resolution and sampling frequency of 2.5 MHz. The overall signal run time of the compensator is 1 μs .

Keywords: hysteresis compensation, modified Prandtl-Ishlinskii method, field-programmable gate array (FPGA)

Introduction

One of the greatest control problems in the application of solid-state actuators lies in the complex hysteresis of the transfer characteristic which exhibits a nonlinear and ambiguous relationship between the output and the input signals of the actuator. In order to master the hysteresis problem, at the beginning of the 1990s an efficient solution was developed which is based on the compensation of the hysteretic nonlinearities by means of inverse hysteresis operators. A method developed for compensating complex hysteretic actuator and sensor characteristics in open loop control is based on the so-called modified Prandtl-Ishlinskii method [1], [2]. An advantage of this theory is that the description of the hysteretic input-output characteristics is of a phenomenological nature and thus completely abstracted from the hysteresis creating physical processes inside the system. Thus, this method is universal, i.e. it is applicable for the mathematical description of many different hysteresis characteristics and is suitable for a wide range of different actuators and sensors.
The implementation of a feed-forward compensator for hysteretic nonlinearities occurs with the application of an inverse modified Prandtl-Ishlinskii hysteresis operator, defined as serial connection of an inverse Prandtl-Ishlinskii superposition operator S^{-1} and an inverse Prandtl-Ishlinskii hysteresis operator H^{-1} by equation

$$\begin{aligned} \Gamma^{-1}[y](k) &= H^{-1}\left[S^{-1}[y]\right](k) \\ &= \sum_{i=0}^{n} w'_{Hi} H_{r'_{Hi}}\left[\sum_{i=-l}^{+l} w'_{Si} S_{r'_{Si}}[y], z'_{H0i}(r'_{Hi})\right](k) \end{aligned} \quad (1)$$

with the threshold values r'_{Hi}, the weights w'_{Hi}, the initial values z'_{H0i} of the hysteretic memory and with the elementary components $H_{r'_{Hi}}$, i=0..n, for the creation of the inverse Prandtl-Ishlinskii hysteresis operator as well as with the threshold values r'_{Si}, the weights w'_{Si} and with the elementary components $S_{r'_{Si}}$, $i=-l..+l$, for the creation of the inverse Prandtl-Ishlinskii superposition operator [1], [2]. Thus, the hardware structure of the inverse filter for a digital implementation is to be seen in Fig. 1. This realisation consists of two stages, the first describes the inverse Prandtl-Ishlinskii superposition operator, the second the inverse Prandtl-Ishlinskii hysteresis operator, in which the initial values z'_{H0i}, i=0..n, are set to zero.

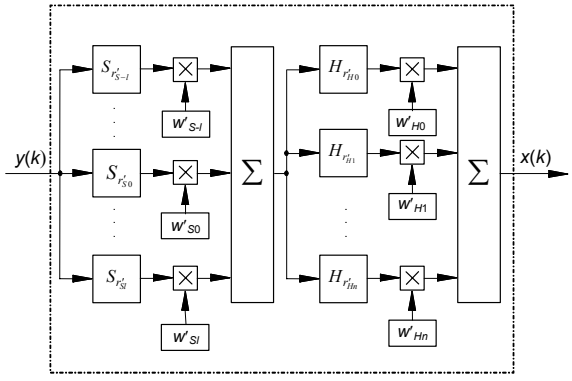

Fig. 1: *Hardware structure of the compensator*

The paper will first show the problem statement of compensating hysteretic nonlinearities for highly dynamic applications. Thereafter the design of a stand-alone hysteresis compensation module based on FPGA [5c], the complete approach for FPGA programming and final results are presented.

Problem statement

In practice, the effectiveness of the compensation effect depends strongly on the rate independence property of the compensator in the operating frequency range of the application. In a time-discrete implementation of the control algorithm primarily the antialiasing and reconstruction filters in the A/D and D/A converter circuits but also the time delays in connection with the calculation of the control algorithms as well as the A/D and D/A conversion result in frequency dependent phase errors which contribute considerably to an unwanted rate dependence of the compensator already at low sampling frequencies. To go into details, we consider a general structure of a sampling system (see Fig. 2), consisting of three main parts, namely signal digitalisation, signal processing (SP) and signal reconstruction.

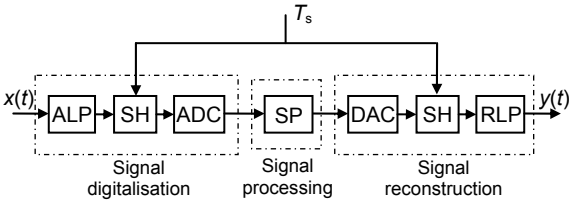

Fig. 2: *General structure of a sampling system*

The signal digitising and signal reconstructing blocks each contain a sample and hold circuit (SH), a low-pass filter (ALP and RLP), which is implemented as a third-order Butterworth low-pass filter defined by the transfer function

$$G_{\mathrm{ALP}}(p) = G_{\mathrm{RLP}}(p) = \frac{1}{\left(\frac{p}{\omega_{\mathrm{g}}}\right)^3 + 2\left(\frac{p}{\omega_{\mathrm{g}}}\right)^2 + 2\left(\frac{p}{\omega_{\mathrm{g}}}\right) + 1} \qquad (2)$$

in the Laplace domain with the complex frequency $p = \sigma + \mathrm{j}\omega$ and the -3 dB cut-off frequency ω_{g} as well as an A/D or D/A converter, respectively. The signal processing part has a time delay behaviour defined by the transfer function

$$G_{\mathrm{SP}}(p) = \exp(-pT_{\mathrm{s}}) \qquad (3)$$

with the sampling period T_{s}. Fig. 3 presents the corresponding amplitude and phase responses of the transfer functions G_{ALP}, G_{SP} and G_{RLP}.
According to the Nyquist theorem [4] the minimum sampling frequency f_{s} should be equal to

$$f_{\mathrm{s}} = 2f'_{\mathrm{y}}, \qquad (4)$$

f'_{y} is the highest signal frequency component of the input signal $y(t)$ (in this case f'_{y} is the frequency corresponding to -60 dB damping), see Fig. 3. The time delays in the digital signal processing unit and, mainly, the phase shifts caused by the low-pass filters negatively affect the performance of the overall system. This effect can be seen in the form of the deviation from the ideal linear transfer behaviour $y = x$ as seen in Fig. 4 for

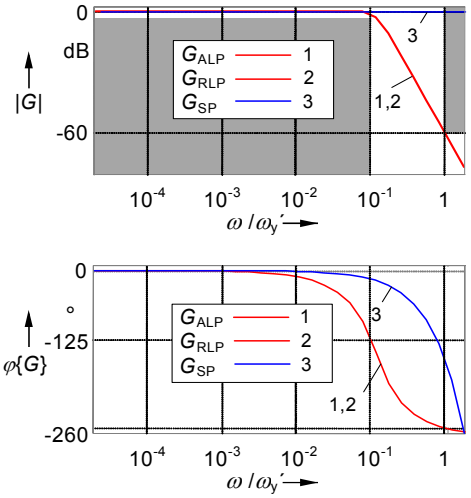

Fig. 3: *Amplitude and phase responses*

the antialiasing low-pass filter (left), for the SP (right) and the entire system transfer function including reconstruction low-pass filter (bottom).

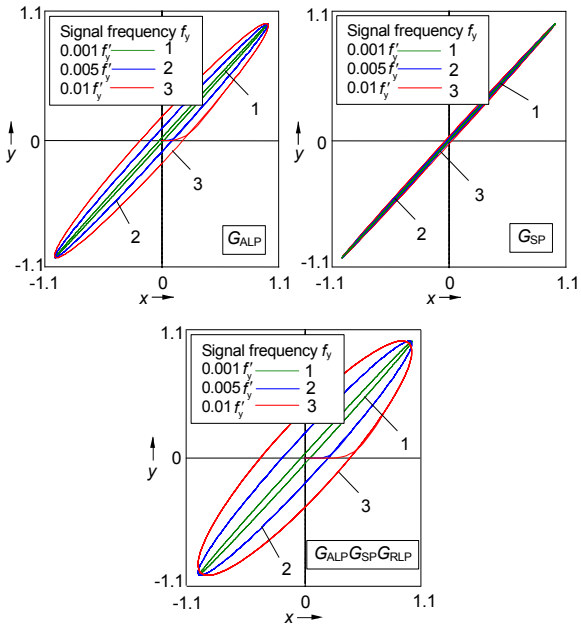

Fig. 4: *Errors due to time delay and phase-shift problems in sampling systems*

To avoid large time delay and phase shift errors, the maximum signal frequency f_{y} of the real input signal $y(t)$ should be less than 0.001 f'_{y} (see curve 1), meaning that the sampling frequency f_{s} should be around the factor 2000 greater than the highest signal frequency component f'_{y}. Hence, vibration control applications with signal frequencies up to 1 kHz for example are not feasible on the basis of microcontrollers or DSPs. To achieve hysteresis compensation in high-speed applications, an alternative approach which is based on a hardware implementation of the hysteresis compensator using a FPGA [5c] has been realised at the LPA. This execution in which the algorithms based on the modified Prandtl-Ishlinskii method can be implemented with a high degree of parallelity

allows sampling frequencies in the megahertz range.

Design of stand-alone hysteresis compensation module

Fig. 5 presents the schematic diagram of a stand-alone hysteresis compensation module consisting of two input channels V_{in1}, V_{in2} and two output channels V_{out1}, V_{out2}.

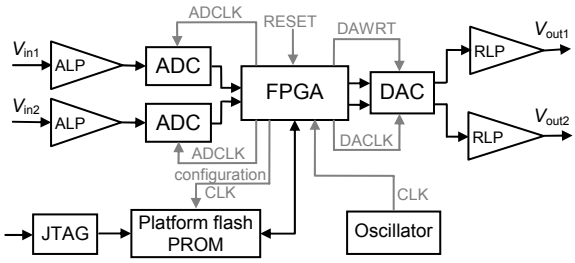

Fig. 5: *Schematic diagram of stand-alone hysteresis compensation module*

The input channels are comprised of an antialiasing low-pass filter (ALP) with a cut-off frequency adjusted to 130 kHz and a 14 bit analogue-to-digital converter (ADC) for digitising the input signal with the sampling frequency of 2.5 MHz. The output channels are responsible for digital-to-analogue conversion (DAC) with the 14 bit resolution and the following low-pass filtering (RLP) with a cut-off frequency of 130 kHz for reconstructing the continuous output signal. In addition, the module contains a platform flash PROM for storing the FPGA configuration data. The configuration data are downloaded via the JTAG interface from the computer onto the platform flash PROM and stored. After power-up or reconfiguration the FPGA automatically loads the configuration bitstream in bit-serial form from the flash PROM synchronized by the configuration CLK generated by the FPGA. With the help of the state machines programmed in the FPGA the respective clock signals for the A/D (ADCLK) and D/A (DAWRT, DACLK) converters are generated by the FPGA from the oscillator clock signal CLK of 10 MHz. The appropriate timing diagrams are to be seen in Fig. 6.

Comments on Fig. 6:

1. Data transfer to A/D converter
2. End of conversion, data transfer to FPGA
3. At this point the FPGA is finished with the calculations (according to investigations the FPGA needs 125 ns for the calculation, i.e. we have a time reserve of 275 ns to implement the other calculating algorithms in FPGA)
4. Data output from FPGA
5. Data transfer to D/A converter
6. Data output from D/A converter

Therewith the overall signal run time of the compensator amounts 1 µs.

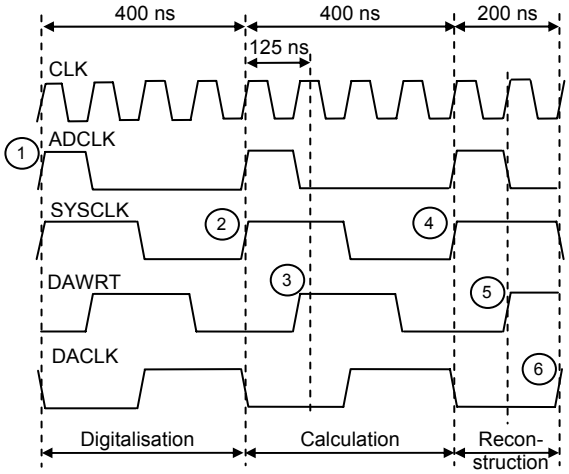

Fig. 6: *Timing diagrams: clock signals*

Fig. 7 shows the FPGA adapter board. On this eight layer card with the mechanical dimensions of 80 × 120 × 1.5 mm^3 are placed the FPGA (a) together with the platform flash PROM (b), oscillator (on the bottom side) as well as A/D (c) and D/A (d) converters. The adapter contains four 50-pole strips (e) to which 200 FPGA I/O-pins are connected. Using the DIP switch (f) the oscillator frequency can be set to 100 kHz, 1 MHz or to 10 MHz. Via the 14-pole connector (g) the configuration data are downloaded onto flash PROM.

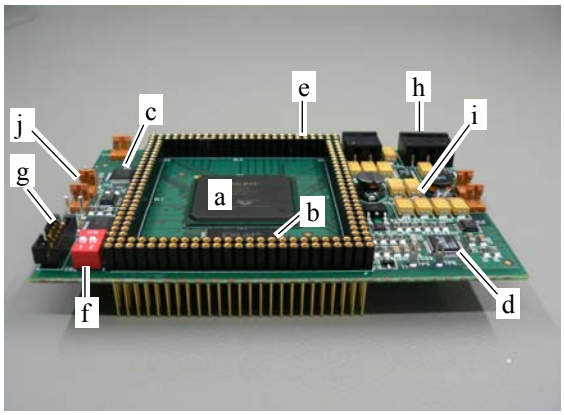

Fig. 7: *FPGA adapter board*

The 3-pole screw connector (h) is used for the external power supply voltage of ±5 V and with the power supply unit (i) placed on this board all required voltages for all devices are generated from it. The 2-pole PCB connectors (j) are planned for the signal lines routed from the main board implemented as a Euro card (100 × 160 × 1.5 mm^3). On this main board are placed a third-order Butterworth antialiasing input and a reconstruction output low-pass filter. These both boards compose the entire design of a stand-alone hysteresis compensation module.

Complete approach for FPGA programming

In this section the complete approach for the FPGA programming is presented according to the schematic diagram shown in Fig. 8.

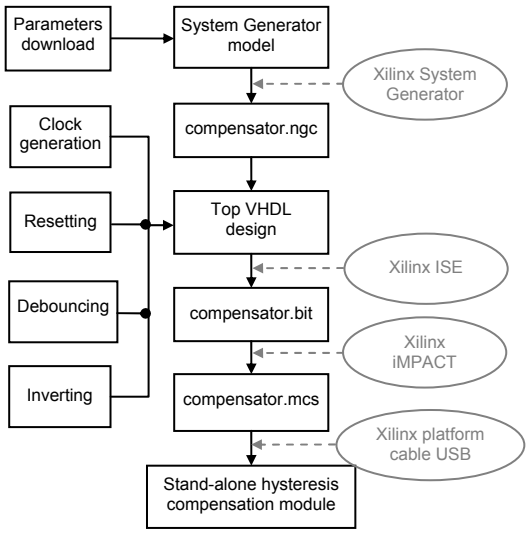

Fig. 8: *Approach for FPGA programming*

At first all required parameters (weights, initial and threshold values) for the inverse modified Prandtl-Ishlinskii hysteresis operator are downloaded into the Matlab environment. With the use of the Xilinx System Generator software [5e] implemented as a Matlab block set, the presented file *compensator.ngc* [5a] is generated in binary form based on the mathematical model for compensating the hysteretic nonlinearities. This file together with four additional VHDL [3] modules, namely

- Clock generation (delivers the clock signals for A/D and D/A converters as well as for FPGA input and output registers, see Fig. 6)
- Resetting (generates the reset signal for the FPGA)
- Debouncing (since a mechanical press switch is planned for reset release, this module serves for debouncing, implemented on the basis of an RS flip-flop from two NAND gates, see [4])
- Inverting (realizes a double inverting of the oscillator signal CLK to make its edges steeper)

are added as single components to the top VHDL design created in the Xilinx ISE software [5a].
Using this software one explains all necessary processes beginning with synthesis up to place and route for the top VHDL design and generates afterwards the bitstream file *compensator.bit*. With the Xilinx iMPACT software [5d] the *bit* format file is converted into the PROM file *compensator.mcs* which is compatible with the Xilinx platform flash PROMs. Subsequently, this file can be downloaded via the Xilinx platform cable USB [5b] onto the platform flash PROM located on the stand-alone hysteresis compensation module. The system is then ready for use.

Results

The two-channel FPGA module can compensate two complex hysteretic actuator characteristics independently and simultaneously in open-loop control, or one inverse filter can be integrated in a closed control loop, i.e. the second channel can be used for the feedback implementation. This module is easily extendable to several channels, since the FPGA works below its full capacity, i.e. other control algorithms could be implemented in the FPGA. According to investigations up to 5 parallel channels can be realised, i.e. up to 5 actuators can be driven at the same time with the module. This corresponds with 85% of full capacity of the FPGA chip.
As a result Fig. 9 represents the linearization (curve 4) of the hysteretic nonlinearity W as curve 1 (in gray), reproduced by the modified Prandtl-Ishlinskii hysteresis operator Γ as curve 2 (in black) with the application of the compensator Γ^{-1} as curve 3 for a magnetostrictive actuator.

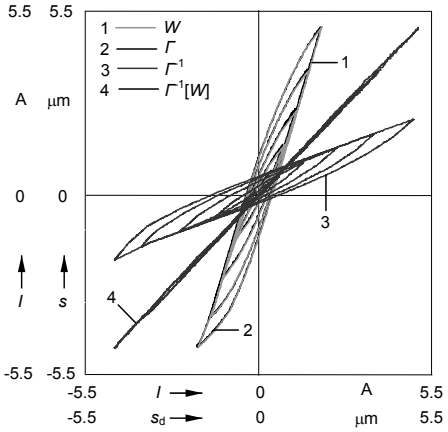

Fig. 9: *Hysteresis modelling and compensation*

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